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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte GEORGE SAPNA and HAIYUN YANG

Appeal 2009-0411
Application 09/486,582
Technology Center 2600

Decided:[1] May 11, 2009

Before KENNETH W. HAIRSTON, MARC S. HOFF,
and KARL D. EASTHOM, *Administrative Patent Judges*.

EASTHOM, *Administrative Patent Judge*.

DECISION ON APPEAL

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[1] The two month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, begins to run from the decided date shown on this page of the decision. The time period does not run from the Mail Date (paper delivery) or Notification Date (electronic delivery).

STATEMENT OF CASE

Appellants appeal under 35 U.S.C. § 134 from final rejections of claims 1-20. No other claims are pending. (App. Br. 2). We have jurisdiction under 35 U.S.C. § 6(b).

We affirm.

Appellants' invention decodes a compressed audio bitstream to produce a digital audio output, employing an algorithm mathematically operating on arrays of data. The decoding operation can be implemented by computer software and/or hardware. The decoding algorithm calls for producing sums and differences of the input data and then multiplying the sums and differences by coefficients. (Spec. 2:8-29; 12:6-10).

Independent claims 1, 8, 11, and 14, representative of the claims on appeal, read as follows:

> 1. A method of decoding digital audio data, comprising the steps of:
>
> obtaining an input sequence of data elements representing encoded audio samples;
>
> preprocessing the input sequence of data elements to produce an array of sum data and an array of difference data using selected data elements from the input sequence;
>
> producing a first sequence of output values using the array of sum data;
>
> producing a second sequence of output values using the array of difference data; and
>
> forming decoded audio signals from the first and second sequences of output values.

8. A method of decoding a sequence of m, m an even positive integer, input digital audio data samples S[k], where k = 0, 1, ... (m-l), to produce a set of n, n an even positive integer, output audio data samples V[i], where i = 0, 1, ...(n-l), comprising the steps of:

a) producing an array of sum data $S_{ADD}[k]$ according to

$$S_{ADD}[k] = S[k] + S[m-l-k] \text{ for } k = 0, 1, ...(m/2-1)$$

b) producing an array of difference data $S_{SUB}[k]$ according to

$$S_{SUB}[k] = S[k] - S(m-l-k) \text{ for } k = 0, 1, ...(m/2-1)$$

c) producing a first output audio data sample by a multiply-accumulate operation according to

$$V[2i] = V[2i] + N[i, k]*S_{ADD}[k] \text{ for } k = 0, 1, ... (m/2-1)$$

$$\text{where } N[i, k] = \cos\{[(32 + 2i)(2k + 1)\pi]/64\}$$

d) producing a second output audio data sample by a multiply-accumulate operation according to

$$V[2i+1] = V[2i+1] + N[i, k]*S_{SUB}[k] \text{ for } k = 0, 1, ... (m/2-1)$$

$$\text{Where } N[i, k] = \cos\{[(32 + (2i + 1))(2k + 1)\pi]/64\}$$

e) and repeating steps c) and d) for i = 0, 1, ... (n/2-1) to produce a full set of output data.

11. A synthesis sub-band filter for use in decoding digital audio data, comprising:

means for receiving or retrieving an input sequence of data elements comprising encoded digital audio data;

pre-processing means for producing an array of sum data and an array of difference data using selected data elements from the input sequence; and

transform output means for producing a first sequence of decoded output values using said array of sum data and a second sequence of decoded output values using said array of difference data.

14. An MPEG decoder comprising:

means for receiving an input sequence of data elements comprising encoded digital audio data;

means for producing an array of sum data and an array of difference data using selected data elements from the input sequence; and

means for producing a first sequence of decoded output values using said array of sum data and a second sequence of decoded output values using said array of difference data.

The Examiner relies on the following prior art references:

Uramoto EPO 0506111 A2 (Sept. 30, 1992)

International Standard ISO/EIC 11172-3, Information Technology – Coding of Moving Pictures and Associated Audio for Digital Storage Media at up to About 1.5 Mbit/s – Part 3: Audio, pp. 36, 41 (1st ed., Aug. 1, 1993) ("ISO Standards").

Discrete Cosine Transform, http://en.wikipedia.org/wiki/Discrete_cosine_transform (last visited Nov. 27, 2007).

Claims 1-20 stand rejected under 35 U.S.C. § 101 as being directed to non-statutory subject matter.

Claims 1-6, 11, 18, and 19 stand rejected under 35 U.S.C. § 103(a) as being obvious based on Uramoto.

Claims 7-10, 12-17, and 20 stand rejected under 35 U.S.C. § 103(a) as being obvious based on Uramoto and the ISO Standards.

ISSUES

Appellants' arguments and the Examiner's findings present the following two issues:

Does each independent claim define either a patent-eligible machine or process as required under 35 U.S.C. § 101?

Did Appellants demonstrate, under 35 U.S.C. § 103(a), that the Examiner erred in finding that Uramoto, or Uramoto in combination with the ISO Standards, teaches producing an array of sum and difference data using selected data elements from the input sequence, as set forth in the claims?

35 U.S.C. § 101 STATUTORY SUBJECT MATTER

Principles of Law

35 U.S.C. § 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Under 35 U.S.C. § 101, four categories of subject matter are eligible for patent protection: (1) processes; (2) machines; (3) manufactures; and (4) compositions of matter. "A claimed process is surely patent-eligible under § 101 if: (1) it is tied to a particular machine or apparatus, or (2) it transforms a particular article into a different state or thing." *In re Bilski*, 545 F.3d 943, 954 (Fed. Cir. 2008) (en banc). "Transformation and reduction of an article 'to a different state or thing' is the clue to the patentability of a process claim that does not include particular machines." *Gottschalk v. Benson*, 409 U.S. 63, 70 (1972).

This machine-or-transformation test for processes was reaffirmed recently in *In re Comiskey*, 554 F.3d 967, 978 (Fed. Cir. 2009) ("*Comiskey II*") (*revising In re Comiskey*, 499 F.3d 1365 (Fed. Cir. 2007) ("*Comiskey I*") (*vacated & reh'g granted, In re Comiskey* __ F.3d ___, 89 USPQ 2d 1641 (Fed. Cir. 2009) (en banc)), and in *In re Ferguson*, ___ F.3d___, 2009 WL 565074 at *3, No. 2007-1232 (Fed. Cir. Mar. 6, 2009) ("We stated that the Supreme Court's machine-or-transformation test is the 'definitive test to determine whether a process claim is tailored narrowly enough to encompass only a particular application of a fundamental principle rather than to pre-empt the principle itself.'") (quoting *Bilski*, 545 F.3d at 954).

Comiskey II, 554 F.3d at 978, cites and describes Supreme Court and Federal Circuit precedent as requiring, for computer type processes reciting algorithms, processes that "otherwise involve[] another class of statutory subject matter." "For example, we have found processes involving mathematical algorithms used in computer technology patentable because they claimed practical applications and were tied to specific machines." *Id.*

at 979; *see id.* at 979 n.14 (citing cases, describing *Arrhythmia Research Tech., Inc. v. Corazonix Corp.*, 958 F.2d 1053, 1058-59 (Fed. Cir. 1992) as "holding patentable a method for analyzing electrocardiograph signals for the detection of a specific heart condition that used 'electronic equipment programmed to perform mathematical computation,'" and quoting *In re Alappat*, 33 F.3d. 1526, 1544 (Fed. Cir. 1994) ("This is not a disembodied mathematical concept which may be characterized as an 'abstract idea,' but rather a specific *machine* to produce a *useful*, concrete, and tangible *result*.") (emphasis added by *Comiskey II*)).

Despite *Alappat*'s "useful, concrete, and tangible result" language emphasized in part by *Comiskey II*, *supra*, *Bilski* did not rely on that test, according to *Ferguson*: "The decisions of the Board and the briefing and argument on appeal include extensive discussion of a so-called 'useful, concrete, and tangible result' test. To avoid confusion, we clarify here that in *Bilski*, this court considered whether this 'test' is valid and useful and concluded that it is not." *Ferguson*, 2009 WL 565074 at *4.

Regardless of the claim form, claims involving computer algorithms cannot pre-empt the use of a fundamental principle. *See Bilski*, 545 F.3d at 954 ("The question before us then is whether Applicants' claim recites a fundamental principle and, if so, whether it would pre-empt substantially all uses of that fundamental principle if allowed."); *Allapat*, 33 F.3d at 1544 ("Indeed, claim 15 as written is not 'so abstract and sweeping' that it would 'wholly pre-empt' the use of any apparatus employing the combination of mathematical calculations recited therein.") (*quoting* Benson, 309, U.S. at 68-72).

Finally, according to USPTO guidelines, claims must be amended to recite solely statutory subject matter.[2]

Claims 1-7, 18, and 19 (process claims)[3]

Findings of Fact (FF)

1. Appellants describe their invention as follows:

> In accordance with the present invention there is provided a method of decoding digital audio data, comprising the steps of obtaining an input sequence of data elements representing encoded audio samples, calculating an array of sum data and an array of difference data using selected data elements from the input sequence, calculating a first sequence of output values using the array of sum data, calculating a second sequence of output values using the array of difference data, and forming decoded audio signals from the first and second sequences of output data.

(Spec. 2:23-29).

2. According to Appellants, their invention reduces processing steps:

> Embodiments of the present invention are able to reduce the number of arithmetic operations performed in implementing the IMDCT portion of the decoder, to thereby increase the computational efficiency of the decoding process. In particular, the number of addition operations required for the implementation of this equation can be reduced substantially by pre-computing the sum and difference of the sample data which is the input to the IMDCT.

(Spec. 7:10-15).

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[2] *See* MPEP § 2106(IV)(C)(2)(2)(a), Rev. 6, Sept. 2007 ("MPEP") ("[A] claim that can be read so broadly as to include statutory and nonstatutory subject matter must be amended to limit the claim to a practical application.").

[3] Appellants argue these claims as a group, focusing on claim 1 (App. Br. 5-7). Accordingly, pursuant to 37 C.F.R. § 41.37(c)(1)(vii), claim 1 is selected to represent the group.

3. Appellants also describe their invention alternatively in terms of 1) a general purpose computer with specially adapted software or 2) hardware:

> In any event, it is immediately recognisable [sic] that one way the invention can be carried out, relating as it does to the processing of data, is using general purpose computing apparatus operating under the instruction of software or the like which is produced separately and specially adapted to perform the methods of the invention. Alternatively, specialised [sic] computing apparatus such as a dedicated integrated circuit, chipset or the like may be constructed with the functions of the invention embedded therein.

(Spec. 12:6-12).

4. Appellants provide support (App. Br. 3) for claim 1 based on Figures 3-5 and the last paragraph of page 2 in the Specification. Appellants also generally cite pages 2-12 of the Specification for support. The final step in Figures 3-5 refers to either samples or data. The last paragraph of page 2 refers to "forming decoded audio signals from the first and second sequences" (Spec. 2:29-30; *see* FF 1 *supra*).

5. Appellants do not refer to Figure 2 for support of claim 1. Figure 2 depicts a conventional MPEG decoder hardware circuit. (Spec. 5:3-15).

6. Appellants state: "The decoder . . . accepts the compressed audio *bitstream* in the defined syntax, decodes the data elements and uses the information to produce *digital audio output*, also according to the defined standard (Spec. 2:8-10) (emphasis added).

7. Appellants describe "[t]he syntheses sub-band filter bank" as: "composed of two main functions, an Inverse Modified Discrete Cosine Transform (IMDCT) and an Inverse Pseudo-Quadrature Mirror Filter (IPQMF). The IMDCT, which can be viewed as an overlap transform,

performs a 32 x 64 cosine modulation transformation, which means a frequency shift of a filter bank into one single filter" (Spec. 5:29 to 6:2). Appellants also refer to "[p]rior art implementations of equation 3" (Spec. 7:26). Equation 3, according to Appellants, represents "[t]he IMDCT equation" (*id.* at l.7) as modified by Appellants to perform less MAC (multiply and accumulate) operations on sample data (*id.* at ll.13-30). The prior art IMDCT equation – prior to Appellants' modification – is represented by Equation 1 (Spec. 6).

Analysis

The Examiner found: "There is no practical application by physical transformation present in the claims. Digital audio data is not physical, rather a form of energy representing data. Manipulating this energy does not involve a physical transformation" (Ans. 4). Appellants responded as follows (App. Br. 6): "The Examiner's position has been flatly rejected by the Federal Circuit." To support the response, Appellants (*id.*) rely on and quote *Arrhythmia*, 958 F.2d at 1059 ("The view that there is 'nothing necessarily physical about "signals"' is incorrect.").

Claim 1 involves manipulating or otherwise transforming input digital data. Appellants do not argue that the input or output signal is a time varying analog signal. According to Appellants, the decoder process produces a digital output (FF 6) that saves calculation steps as compared to prior art decoders/transformers (FF 2). It follows that Appellants' output "signals," according to claim 1 ("forming decoded audio signals from the first and second sequences of output values") and Appellants' disclosure,

constitute a mere stream of data values or samples (FF 1-7).[4] The nominal recitation of "audio" samples as an "input sequence of data elements" constitutes non-functional descriptive material since the claimed process operates the same regardless of the type of data involved.[5]

Therefore, Appellants' reliance on *Arrhythmia* is misplaced. In *Arrhythmia*, 958 F.2d at 1059, the court found: "The electrocardiograph signals are first transformed from analog form, in which they are obtained, to the corresponding digital signal. These input signals are not abstractions; they are related to the patient's heart function." As noted *supra*, *Comiskey II* also describes the claimed invention in *Arrhythmia* as tied to a specific machine. Thus, the process claims in *Arrhythmia* embraced both of the machine and transformation prongs of the statutory test for processes as outlined, *inter alia*, in *Benson*, *Ferguson*, and *Comiskey II*. While only one prong is required to pass the test, Appellants' claims satisfy neither.

No physical transformation occurs in Appellants' claimed invention, and the claims are not tied to a specific machine. The data inputs and outputs are digital, as discussed *supra* (FF 1-7). No *Arrhythmia* type of analog to digital or digital to analog signal transformation occurs. *Benson*

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[4] *See also* claim 7, which depends from claim 1, reciting ". . . wherein the decoded audio signals comprise pulse code modulation samples." This further implies that the output of claim 1 comprises digital data.

[5] Non-functional descriptive material cannot render patentable an otherwise unpatentable product or process. *In re Ngai*, 367 F.3d 1336, 1339 (Fed. Cir. 2004); *Ex parte Curry*, 84 USPQ2d 1272, 1275 (BPAI 2005) (Informative Opinion) (*aff'd*, Rule 36, Fed. Cir., slip op. 06-1003, June 2006).

forecloses mere transformation of data as a statutory process, even if a machine is nominally recited.[6]

According to Appellants, the disclosed process is more efficient than prior art processes that first multiply signals by a coefficient, and then subtract the result. Specifically, Appellants' disclosed process subtracts samples S[k] first, and then multiplies the result to obtain N[i, k] S_{SUB}[k] – instead of multiplying first and then subtracting; i.e., NS[k] – NS[m-l-k] (*see* Fig. 5, steps 108, 118; *see also* claim 8; FF 2, 7). Similar calculations involve adding data to obtain S_{ADD} (Fig. 5, step 106). (*See also* Reply Br. 3;[7] FF 2, 7).

Therefore, Appellants' claim 1 is similar to the "improved mathematical method" claims held non-statutory in *Walter*:

> This case is distinguishable from *In re Johnson*, *supra*. There the claims were drawn to the enhancement of digital data in seismic records by removing the noise from the physical signals representing physical phenomena. Mathematics were employed to this end. . . . . Operation of the claimed process in *Johnson converted the noise-containing physical seismic record present at the start to a new record minus the noise component. Here, appellant claims only an improved mathematical method for cross-correlation.*

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[6] *Benson*'s method claim 8 recited a specific machine – a shift register – yet the claim was held nonstatutory. 409 U.S. at 73-74. The claims recited mere data – involving a conversion of binary coded decimal (BCD) to pure binary. *Benson* also recognized that signals constitute energy or matter, but still held claims to a process of such data non-statutory: "The representation of numbers may be in the form of a time series of electrical impulse, magnetized spots on the surface of tapes . . . holes on paper cards, or other devices." *Id.* at 65.

[7] Appellants argue: "In essence, the steps of Uramoto are performed in a different order for a different purpose."

In re Walter, 618 F.2d 758, 770 (CCPA 1980) (distinguishing *In re Johnson*, 589 F.2d 1070 (CCPA 1978)) (emphasis added). Accordingly, Appellants' claim 1, by failing to recite a specific machine, or to physically transform signals (such as the noise reduced signals in *Johnson*), is nonstatutory. Claims 2-7, 18, and 19, not separately argued, fall with claim 1.

Claims 8-10 and 20 (process claims)[8]

Claim 8 neither recites a signal nor a machine. Rather, claim 8 involves the mere calculation of sums and differences of array data (*see also* FF 1-7). For the reasons discussed *supra*, claim 8 is also nonstatutory. Claims 9-10 and 20, not separately argued, fall with claim 8.

Claims 11-17 (means plus function claims)[9]

Findings of Fact (FF)

8. Appellants (App. Br. 4-5) provide the same corresponding structure for claims 11 and 14. Claims 11 and 14 are recited in means plus function format. In particular, each clause of both claims relies, *inter alia*, on Figure 5 of the disclosure. Each step that Appellants rely on in Figure 5, steps 104-122, describes mathematical manipulations or calculations. Appellants do not rely on the final step in Figure 5, "Output sub-band data" (step 124).

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[8] Appellants argue these claims as a group, focusing on claim 8 (App. Br. 7). Accordingly, pursuant to 37 C.F.R. § 41.37(c)(1)(vii), claim 8 is selected to represent the group.

[9] Appellants argue these claims in two groups, 11-13 and 14-17, focusing on independent claims 11 and 14 (App. Br. 7-9). However, the arguments and scope of the claims are similar and overlap. Pursuant to 37 C.F.R. § 41.37(c)(1)(vii), claims 11 and 14 are representative of the two groups, but are treated together where overlaps occur.

9. Appellants' statement of corresponding structure (App. Br. 4) for the first means clause in claim 11 follows: "means for receiving or retrieving an input sequence of data elements comprising encoded digital audio data; (Page 4, first full paragraph; Fig. 2, input to audio decoder circuit 20 and the description thereof on page 5, first full paragraph; Figure 3, step 44; Figure 4, step 84; Figure 5, step 104)." It is not clear from Appellants' format whether or not the different figures/pages are relied on together or in the alternative.

Analysis

While Appellants argue (App. Br. 8) on one hand that "specific software and hardware combinations are described in the specification for performing the recited functions," Appellants on the other hand do not dispute "that claims 11 and 14 would read on a general purpose computer configured to execute software instructions" (Reply Br. 3). Rather, Appellants dispute the Examiner's determination that such general purpose computer claims are nonstatutory, reasoning as follows: "The Federal Circuit has recently taken a contrary position" (*id.*, *citing Comiskey I*). However, as noted *supra*, *Comiskey II* superseded *Comiskey I* and remanded claims therein reciting a "module" and "means for," Comiskey II, 554 F.3d at 981; i.e., "claims combining the use of machines with a mental process claim" according to Appellants (Reply Br. 3). Thus, Appellants' argument based on *Comiskey I* is not persuasive.

Appellants also assert (App. Br. 8) that the claims result in "a physical transformation," are "configured to produce a useful, tangible and concrete result," and are "directed to a specific apparatus." The first argument lacks a

factual foundation. Claims 11 and 14, reciting data transformation, do not result in a physical transformation, as explained above. The second argument lacks legal support. The useful, tangible, and concrete result analysis is no longer viable.[10]

Appellants' third argument is not persuasive of Examiner error. Appellants state that "the invention can be carried out . . . using general purpose computing apparatus operating under the instruction of software" (FF 3), as the Examiner found (Ans. 4), and as Appellants admit (Reply Br. 3). In other words, Appellants' means plus function claims, while supported by a combination of hardware and software, also are supported by software algorithms on a general purpose computer (*see also* FF 1, 2, 6-9).[11]

The claims call for means for receiving an input sequence of encoded data, means for forming an array of sums and differences of the data, and then means for outputting decoded values using the arrays. Thus, the claims are directed toward implementing a very simple algorithm operating on mere data (an algorithm that is much broader than the one disclosed – *compare* Fig. 5; Spec. 3:20 to 4:2).

In *In re Alappat*, 33 F.3d 1526, 1541-42 (1994) (en banc), the claimed invention operated on specific rasterizer waveform data. The court found specific circuit elements ("logic *circuit*," "*barrel shifters*," "*ROM*") to support the means clauses. Addressing the Board's finding that the claims also read on a general purpose computer, the court stated that "[w]e have

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[10] *In re Ferguson*, 2009 WL 565074 at *4 (No. 2007-1232) (Fed. Cir. Mar. 6, 2009) (discussed *supra*).

[11] *See n.2 supra* (claims directed to statutory and non-statutory subject matter must be amended to include only statutory subject matter).

held that such programming creates a new machine, because a general purpose computer in effect becomes a special purpose computer," *id.* at 1545, but the court also found that the claim at issue "unquestionably recites a machine, or apparatus, made up of a combination of known electronic circuitry elements," *id.* at 1541. Thus, the court indicated (either in *dicta* or possibly an alternative holding) that the claims alternatively were directed to a special purpose computer – a specially programmed computer – and embraced statutory subject matter. *Id.* at 1544-45. However, claims 11 and 14 are distinguishable from those involved in *Alappat*.

First, the claims are not limited to any one field. While claim 11 recites: "A . . . filter for use in decoding digital audio data, comprising: means for receiving . . . data elements comprising encoded digital audio data . . .," the filter constitutes a mere mathematical transform/algorithm (FF 3, 7; Fig. 5). While "audio" data is recited, the term "audio" constitutes non-functional descriptive material, as found *supra*.[12] No audio *waveform* data is recited to limit the claim to the specific audio field. Claim 14 does not even recite "audio data," and while it recites an "MPEG decoder" in the preamble, such a decoder merely embraces a software algorithm, for reasons indicated above (*see also* FF 1-3, 6-9).

On the other hand, *Alappat* found that "the preamble specifically recites that the claimed rasterizer converts *waveform* data into output

[12] The type of data constitutes nonfunctional descriptive material for reasons and under factual findings discussed above – the data type does not change the claimed operation. The claim operates similarly on any type of digital data such as video, or any digitized samples of time varying waveforms, such as the samples involved in *Walter*.

illumination data for a display, and the means elements recited in the body of the claim make reference not only to the inputted waveform data recited in the preamble but also to the output illumination data also recited in the preamble." *Alappat*, 33 F.3d at 1544 (emphasis added). Thus, the court concluded that "claim 15 as written is not 'so abstract and sweeping' that it would 'wholly pre-empt' the use of any apparatus employing the combination of mathematical calculations recited therein." *Id.* (citing *Benson*, 409 U.S. at 68-72); *accord Arrhythmia*, 958 F.2d at 1055 (holding process and apparatus claims patentable, apparatus claim 7 reciting, in part, "means for signal averaging a multiplicity of said selected QRS *waveforms*") (emphasis added). In other words, nominal apparatus claims, according to *Alappat* and *Arrhythmia*, require a physical transformation of waveforms limited to a specific field of use in order to avoid pre-empting use of the mathematical principle recited.

The court in *Walter* employed similar reasoning in holding that claims there were not limited to any particular field of use. The preamble in method claim 7 of *Walter* recited, *inter alia*, "seismic waves . . . converted into a corresponding series of digital sample signals," whereas the body of the claim recited "converting said series of sample signals . . . ." 618 F.2d at 761.[13] Despite the recitation of waves and signals, *Walter* concluded that the

[13] The means-plus-function claims in *Walter* were treated as process claims because "the burden must be placed on the applicant to demonstrate that the claims are truly drawn to specific apparatus distinct from other apparatus capable of performing the identical functions." *Walter*, 618 F.2d at 768. *Alappat*, 33 F.3d at 1554-55, citing *inter alia*, *Walter*, held that the Board erred by treating the means plus function claims as process claims, because

preamble only set forth the "environment in which the improvement operates," noting that there was nothing necessarily physical about the "partial product signals" recited in the body of the claim and produced at the output. *Walter*, 618 F.2d at 769-70.

Second, the functions recited in Appellants' claims 11 and 14 are much broader than those involved in *Alappat*. Only a small portion of the disclosed algorithm is required as a means to support such broadly recited functions.[14] Appellants do not clearly limit the means recited to specific circuit elements and indicate that the algorithm itself constitutes the means (*see* FF 8, 9). The recited functions -- receiving encoded input data, producing arrays of sum and difference data, and producing decoded values using the arrays -- can be performed by college mathematics or engineering students working with pen and paper. Such means-plus-function limitations are therefore broad enough to be treated either as embodying a general purpose computer, a process, or a software program on a computer medium (despite the nominal means recitation).[15] Under *Benson*, despite a nominal

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the corresponding claim structure was identified sufficiently with disclosed structure as circuit elements.

[14] "Structural features that do not actually perform the recited function do not constitute corresponding structure and thus do not serve as claim limitations." *Golight, Inc. v. Wal-Mart Stores*, 355 F.3d 1327, 1334-35 (Fed. Cir. 2004) (quoting *Asyst Techs., Inc. v. Empak, Inc.*, 268 F.3d 1364, 1370 (Fed. Cir. 2001).

[15] *Alappat*, 33 F.3d at 1544 n.22, pointed out that "[t]he Board majority . . . failed . . . to point out any particular mathematical equations corresponding to elements (c) and (d) of claim 15." Such is not the case here – all the means recitations correspond to mathematical equations, according to Appellants' described support for the claims (FF 8-9), as implied by

means recitation (i.e., a machine), a claim is non-statutory if it forecloses the practical use of the claimed algorithm.

Three nominal means clauses do not alter the determination that Appellants claim a single *Benson* type algorithm. *Comiskey II*, 554 F.3d at 981, remanded similar claims nominally reciting machines, reasoning in part, *id.* at 979 (quoting *Parker v. Flook*, 437 U.S. 584, 590 (1978)), that "'[a] competent draftsman could attach some form of post-solution activity'" to a claim – i.e., claim a machine. Like Appellants' claims, the claims involved in *Benson* could easily have been modified by inserting "a means for" clause before each step. For example, claim 8 in *Benson* could have been modified as such: *A machine for* "converting signals from binary coded decimal form . . .", comprising: *a means for* "1) storing the binary coded decimal signals . . . ," *means for* "2) shifting the signals . . . ," *means for* "3) masking . . . ," and so on.[16]

Appellants' admissions and disclosure described above (FF 1-7), and under claim analysis principles.

[16] Claim 8 in *Benson* reads as follows:

> The method of converting signals from binary coded decimal form into binary which comprises the steps of
>
> 1) storing the binary coded decimal signals in a reentrant shift register,
>
> 2) shifting the signals to the right by at least three places, until there is a binary '1' in the second position of said register,
>
> 3) masking out said binary '1' in said second position of said register,
>
> 4) adding a binary '1' to the first position of said register,
>
> 5) shifting . . .
>
> 6) adding . . .

The respondents in *Benson* also similarly described their invention as related "'to the processing of data by program'" *Benson*, 409 U.S. at 64, and altered the order of the mathematical steps: "The method sought to be patented varies the ordinary arithmetic steps a human would use by changing the order of the steps." *Id.* at 67.

Therefore, under *Benson*, such nominal means plus function recitations do not save the claims from a determination that such claims would pre-empt the use of the algorithm. "*Indirect attempts* to obtain patents and avoid the rejection, *by drafting claims as a process, or a machine or components* thereof programmed in a given manner, rather than as a program itself, have confused the issue further and *should not be permitted*." *Benson*, 409 U.S. at 72 (quoting the President's Commission on the Patent System) (emphasis added). Even if Appellants' algorithm can be practiced by hand, a claim that "has no substantial practical application except in connection with a digital computer," and claims "a method of programming a general-purpose digital computer to convert signals" would "wholly pre-empt the mathematical formula and in practical effect would be a patent on the algorithm itself." *Id.* at 65, 71-72.

For the reasons stated above, independent claims 11 and 14 do not recite statutory subject matter. Dependent claims 12, 13, and 15-17, not separately argued, fall with the independent claims. Therefore, we will sustain the Examiner's 35 U.S.C. § 101 rejection of claims 11-17.

> 7) shifting the signals to the right by at least three positions in preparation for a succeeding binary '1' in the second position of said register.

Benson, 409 U.S. at 73-74 (internal quotation marks omitted).

OBVIOUSNESS

Principles of Law

"[T]here must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006). "[T]he examiner bears the initial burden, on review of the prior art or on any other ground, of presenting a *prima facie* case of unpatentability." *In re Oetiker*, 977 F.2d 1443, 1445 (Fed. Cir. 1992). "'On appeal to the Board, an applicant can overcome a rejection by showing insufficient evidence of *prima facie* obviousness . . . .'" *Kahn*, 441 F.3d at 985-86 (quoting *In re Rouffet*, 149 F.3d 1350, 1355 (Fed. Cir. 1998)).

> [I]f a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill. . . . [A] court must ask whether the improvement is more than the predictable use of prior art elements according to their established functions.

KSR Int'l Co. v. Teleflex Inc., 550 U.S. 398, 417 (2007). In "difficult . . . cases . . . the claimed subject matter may involve more than the . . . mere application of a known technique to a piece of prior art ready for the improvement." *Id.*

Findings of Fact (FF)

10. Uramoto discloses an IDCT (inverse discrete cosine transform) processor/operation (Uramoto 3:36-39, Equation 2; 10:48 to 12:33; Fig. 11; Abstract). Uramoto's IDCT decoder is similar to the prior art IMDCT

(inverse modified discrete cosine transform) decoder disclosed by Appellants (Equation (1)) and the decoder modified by Appellants (Equation (3)) (*compare id.* with Spec. 6:4 to 7:30; Fig. 5; Equations (1), (3); *see* FF 2, 7).

11. The IDCT decoder of Uramoto's Figure 11 depicts a data rearranging circuit 2, a product sum operation circuit 3, and a post-processing section 7. Circuits 2 and 7 in Figure 11 have the same configurations as circuits 2 and 1 respectively of Figure 4. Circuit 7 also has the same configuration as the more detailed circuits depicted in Figures 5 and 6. (Uramoto 10:53-55; 12:24-26).

12. In Uramoto's IDCT decoder, input data yj (j=0, 1. . . 7) is first input to the re-arranging circuit 2 which re-arranges the data samples so that y0, y2, y4, and y6 are sequentially output, as are data samples y1, y3, y5, and y7 (Uramoto 11:53 to 12:14). The input data yi are then transformed by multiplying and adding (*see* the matrices at Uramoto 11, expression 13 (selected input data yi are multiplied by selected cosine and sine coefficients A-E in circuit 3 and then added to form intermediate terms Mi and Ni)). The intermediate terms for x2, for example, M2 = Ay0 – Cy2 –Ay4 + By6, and N2 = Fy1 – Dy3 + Gy6[sic y5] + Ey7, are produced prior to the post-processing section 7 (Uramoto 12:7-13, *compare* expression 13). Post-processing section 7 then produces sums and differences of the intermediate inputs Mi, Ni, to form the outputs: xi = Mi + Ni (i= 0,1,2,3) and xi = Mi – Ni (i= 4, 5,6,7). (Uramoto 10:48 to 12:33). The sums and differences in section 7 are produced in adder 22 and subtractor 23 after processing by

input circuit 21, and then output at circuit 24 (*see* Fig. 5 – corresponding to post-processing circuit 7 as outlined above (FF 11)).

13. Uramoto discloses that the "only . . . difference between the DCT [encoding] operation and the IDCT [decoding] operation is a difference between coefficients A and A'. Thus, in the configuration of Fig. 1, the IDCT operation can be carried out by changing the coefficients in parallel multipliers 101a-101h." (Uramoto 3:36-39; *see also* 12:31-32).

14. Uramoto discloses that the encoder adder 22 and subtractor 23 in pre-processing circuit 1 pre-process selected data to form intermediate data x0 + x7, x1 + x8, x2 +x5, x3 +x4, and x0-x7, x1-x6, x2-x5 and x3-x4. That data is then sent to multipliers, represented by the matrices appearing in relation 6, resulting in less multiplying in Uramoto's encoder, as compared to the encoder represented by relation 5. (Uramoto 6:54 to 8:34).

15. The ISO Standards document discloses an IMDCT audio cosine decoder/transformer that is similar to the prior art IMDCT cosine transformer disclosed by Appellants (Equation 1) and modified by Appellants (Equation 3) (*compare* ISO Standards 36 *with* Spec., Equations 1, 3; *see also* FF 10).

Analysis

Appellants' assertion (App. Br. 10-13) with respect to claims 1-6, 11, 18, and 19[17] that Uramoto's IDCT (inverse discrete cosine transform) circuit

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[17] Appellants argue claims 1-6, 11, 18, and 19 as a group (App. Br. 10-13), focusing on claims 1 and 11. The nominal recitations (*id.* at 10-11) of elements in claims 1 and 11 do not constitute separate patentability arguments for the two claims. Accordingly, pursuant to 37 C.F.R. § 41.37(c)(1)(vii), claim 1 is selected as representative.

does not produce an array of sum and difference data using selected data elements from the input sequence is not persuasive. M2 and N2 are each composed respectively of selected input data elements y0, y2, y4, y6, and y1, y3, y5, y7 (FF 12). That is, due to the signs of the cosine coefficients A-E, intermediate values, Mi, Ni, also each constitute an array (albeit a single row array) composed of sums and differences of selected input data elements yi. Therefore, M2 includes a first sequence of output values using an array of sum data and N2 includes a second sequence using an array of difference data. The arrays Mi and Ni are used as inputs to the adder 22 and subtractor 23 of Figure 5 to produce decoded audio signals. (FF 11, 12).

Appellants' argument that Uramoto's output (x2 = M2 + N2 = Ay0 - Cy2 - Ay4 + By6 + Fy1 - Dy3 + y5 + Ey7) is not comprised of selected elements from the input sequence, because x2 comprises additions and subtractions of products of input data (App. Br. 12), also is not persuasive. Additions and subtractions of input data do not preclude additions and subtractions of products of such data. The input data is pre-processed (re-arranged) to form the desired values, as the Examiner generally found (Ans. 5, 6, 17, 18); i.e., the re-arranging circuit determines which input data will be multiplied by which transform products and which data values will be added or subtracted together (FF 11, 12).

Appellants' data is also pre-processed before it is processed in Appellants' sub-band filter at step 53, where adding, subtracting, and multiplying occur (Spec. 5:24-27; Fig. 3). Therefore, Appellants' argument (App. Br. 11) that Uramoto's data is intermediate data and not input data, and therefore Uramoto teaches away from the invention, is not persuasive.

Accordingly, Appellants have not demonstrated that the Examiner erred with respect to claim 1, nor claims 2-6, 11, 18, and 19, not separately argued.

With respect to claims 7-10, 12-17, and 20,[18] Appellants rely on similar arguments presented for claim 1, and also assert that Uramoto teaches away from the ISO Standards' IMDCT decoding process, which Appellants refer to as an inverse modified discrete cosine transform process (IMDCT) (App. Br. 13-15). The Examiner points to the ISO Standards (Ans. 10, 11) as teaching an audio IMDCT equation/decoder (FF 15). Appellants admit that Equation 1, representing a form of the IMDCT equation/decoder, was known in the art (FF 2, 7, 10). Uramoto, the ISO Standards, and Appellants disclose decoders that all involve similar cosine transformations (*see* FF 2, 7, 10, 15). Appellants fail to point to any difference between any of the transformers/decoders in terms of claim limitations that support the argument that Uramoto teaches away from the ISO Standards decoder. Employing one or the other similar decoding algorithms, both involving discrete cosine transforms (i.e. multiplying coefficients), amounts to the predictable substitution of prior art elements or methods and their respective functions. *See* KSR, 550 U.S. at 417.

Appellants further assert (App. Br. 14) with respect to claim 8 that M and N do not correspond to S_{ADD} and S_{SUB}. The argument fails to address

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[18] Appellants nominally argue (App. Br. 13-15) claims 7, 12, and 13; 8-10 and 20; and 14-17 as three separate groups, but rely on arguments for claim 1. Appellants' arguments also do not rely on any particular limitations unique to each group, except for limitations recited in claim 8. Thus, pursuant to 37 C.F.R. § 41.37(c)(1)(vii), claim 8 is selected to represent claims 8-10 and 20 and claim 14 is selected to represent claims 7, 12, 13 and 15-17.

the Examiner's finding, supported by the record, that Uramoto discloses the encoder input data terms S_{ADD} and S_{SUB}, respectively, as x0 + x7, x1 + x6 . . ., and x0 - x7, x1- x6, etc. (Ans. 9, 10; FF 14). Uramoto also specifically teaches that adding and subtracting first creates more efficient processing by decreasing multiply steps (FF 14). Uramoto further teaches that the same processes generally can be employed in decoders and encoders – with the coefficient values constituting the central difference between the two (FF 13). Therefore, the record supports the Examiner's finding that Uramoto suggests adding and subtracting selected data elements and then performing the multiply-accumulate operations set forth in claim 8, and also as set forth in claim 14 (i.e. producing sum and difference arrays and decoded values). Accordingly, Appellants did not demonstrate that the Examiner erred in rejecting in rejecting claims 8 and 14, nor of claims 7-10, 12-17, and 20, not separately argued.

Appellants' general assertion (Reply Br. 3), presented for the first time in the Reply Brief,[19] that the claims call for a different order in steps than that of Uramoto, even if it were timely, fails to show error in the Examiner's findings. Appellants' argument reduces to the assertion that adding and subtracting before multiplying constitutes an unobvious step.

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[19] By not timely presenting these arguments in the Appeal Brief, they are deemed waived. *See Optivus Tech., Inc. v. Ion Beam Appl'ns S.A.*, 469 F.3d 978, 989 (Fed. Cir. 2006) ("[A]n issue not raised by an appellant in its opening brief . . . is waived.") (citation and internal quotation marks omitted); *accord Ex Parte Scholl*, No. 2007-3653 (BPAI Mar. 13, 2008) (Informative), at 18-19, *available at* http://www.uspto.gov/web/offices/dcom/bpai/its/fd073653.pdf.

Such a step involves the distributive property, a well-known fundamental mathematical principle.

Further, as discussed above, Uramoto teaches using the same process in decoders and encoders, and suggests adding and subtracting before multiplying in transform based decoders involving such mathematical processing, in order to minimize the number of multiplying steps (FF 13, 14). Accordingly, for these additional reasons, Appellants did not demonstrate that the Examiner erred in rejecting claims 1-20.

CONCLUSION

Each independent claim as a whole defines neither a patent-eligible machine nor a process as required under 35 U.S.C. § 101.

Appellants did not demonstrate, under 35 U.S.C. § 103(a), that the Examiner erred in finding that Uramoto, or Uramoto in combination with the ISO Standards, teaches producing an array of sum and difference data using selected data elements from the input sequence as set forth in the claims.

DECISION

We affirm the Examiner's decision rejecting claims 1-20.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

babc

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